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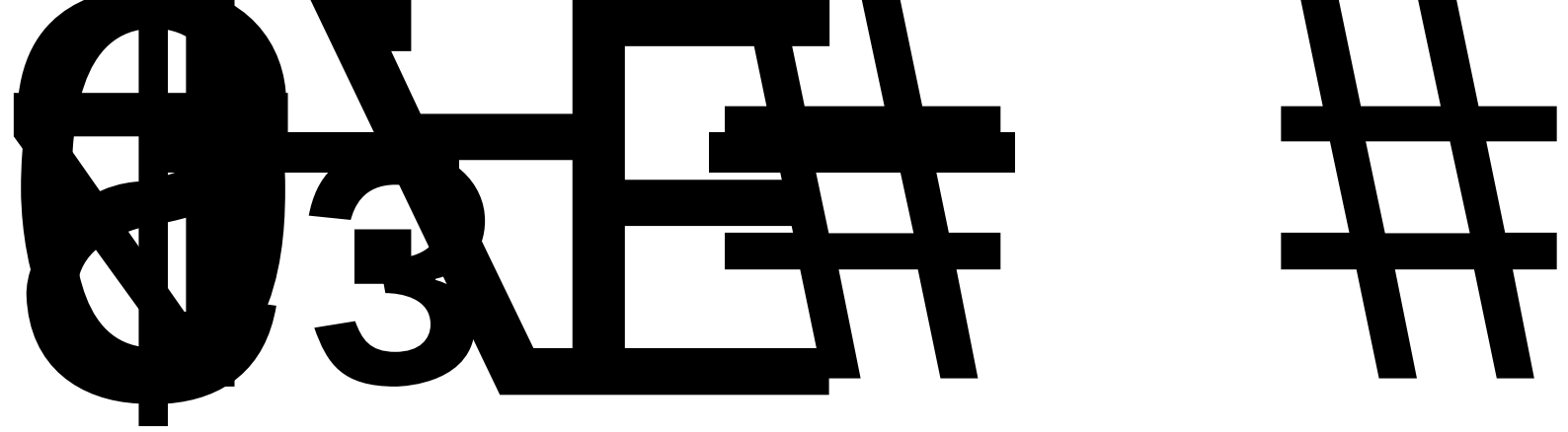
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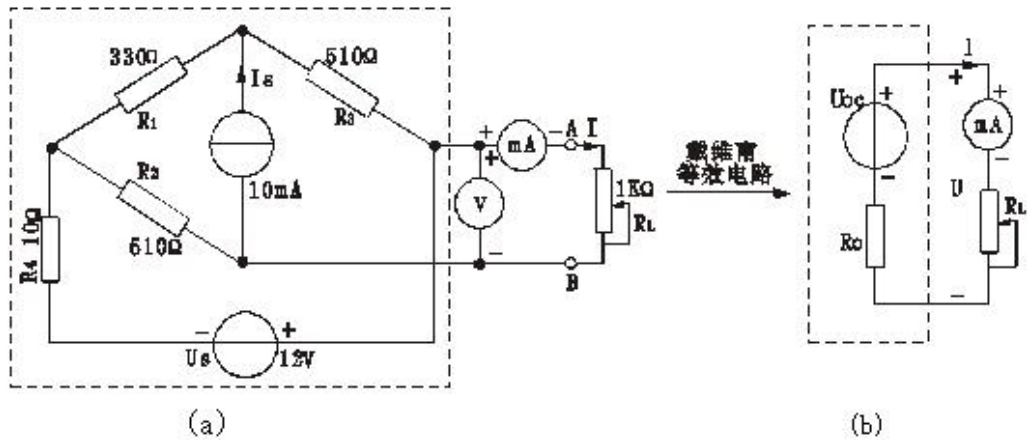
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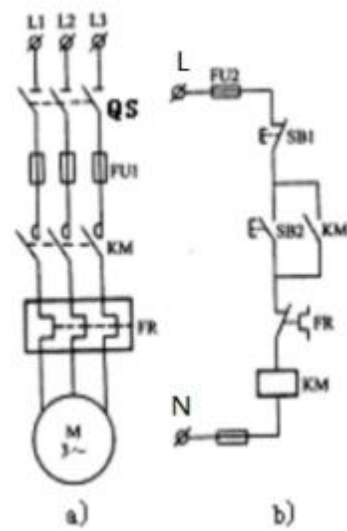
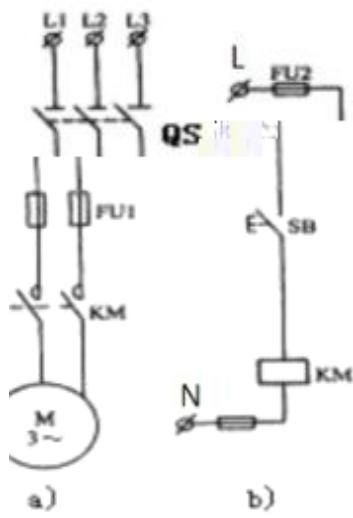
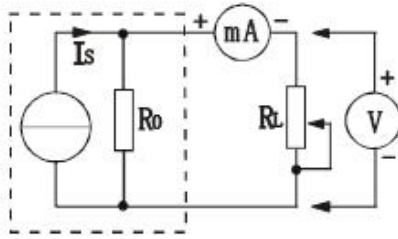
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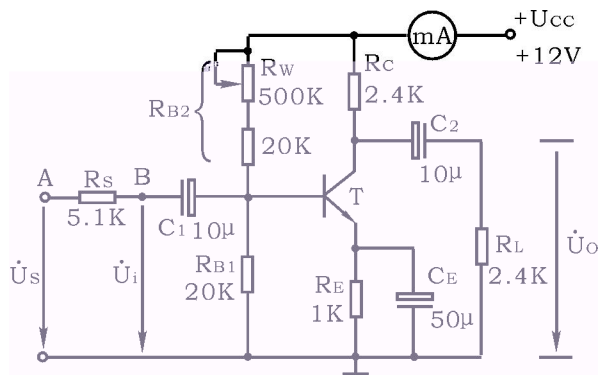
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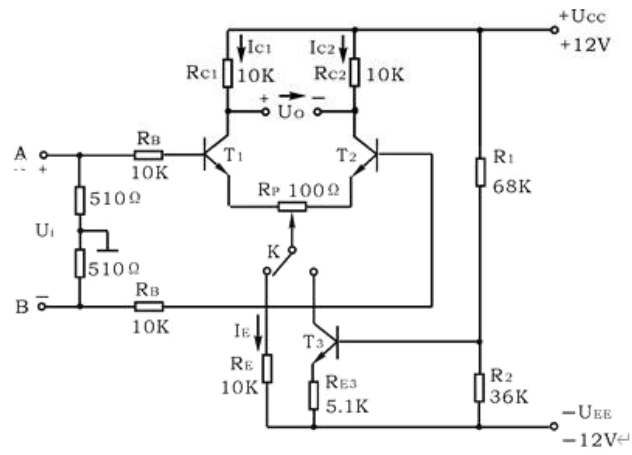


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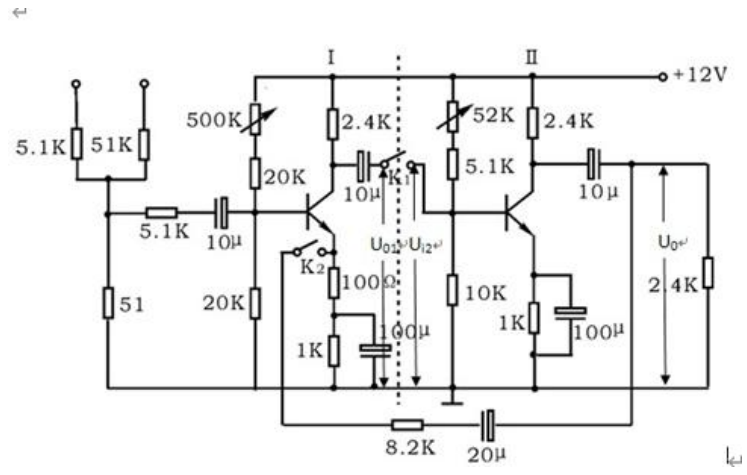


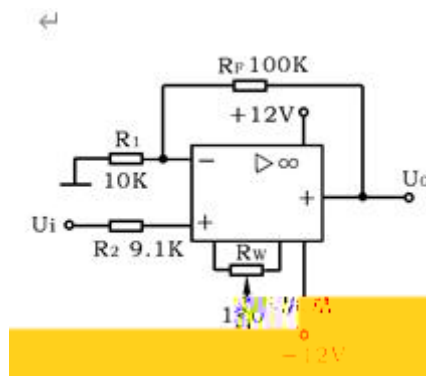
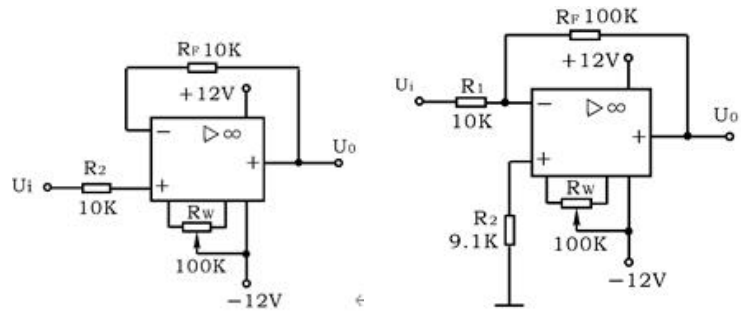
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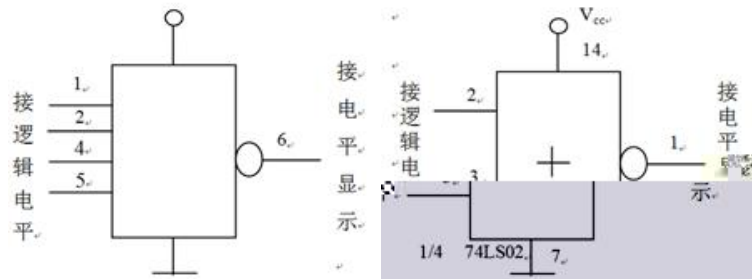
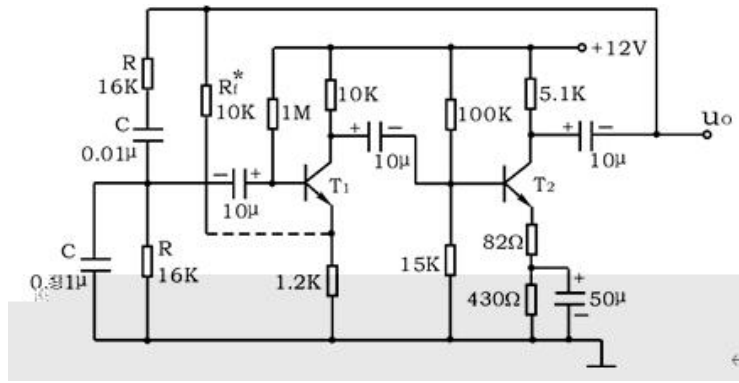


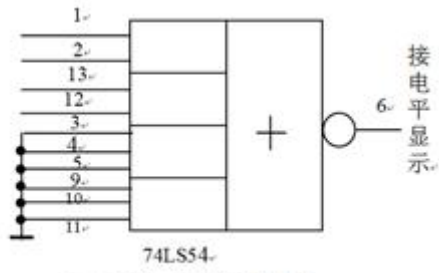
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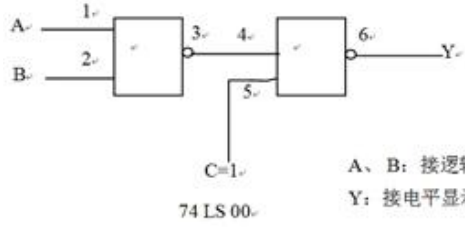




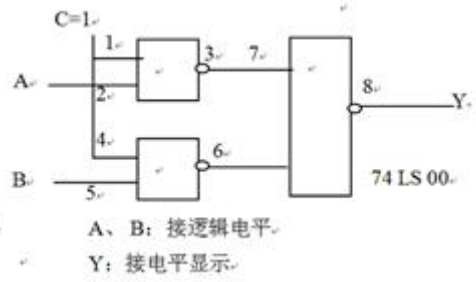




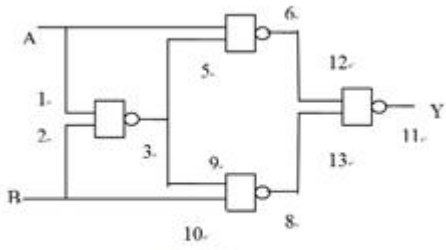
1、2、12、13：接逻辑电平。



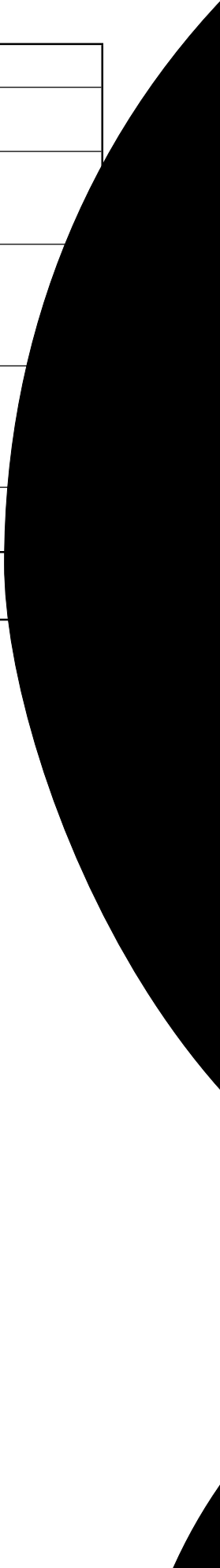
A、B: 接逻辑电平
Y: 接电平显示



A、B: 接逻辑电平
Y: 接电平显示



A、B 接逻辑电平
Y: 接电平显示



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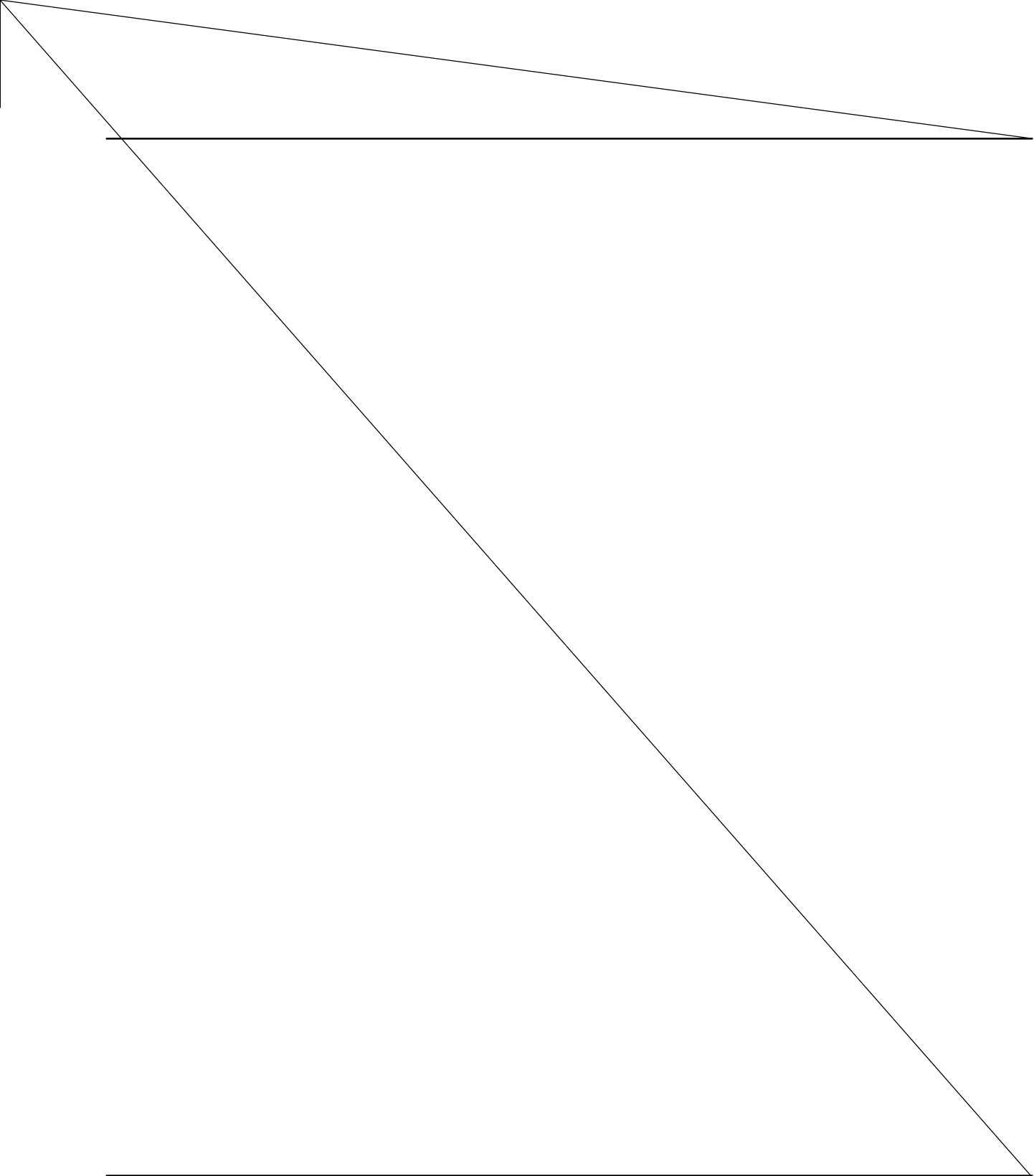
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